# Translation of automotive module RF immunity test limits into equivalent IC test limits using S-parameter IC models

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***Abstract*—A method to translate immunity specifications of automotive modules into equivalent requirements at integrated circuit (IC) level, using linear scattering parameter models of the ICs, is presented. A technique is described to determine S-parameters of ICs by simulations based on back-annotated analog schematics. The simulation results are compared with measurement data obtained using a specially designed test board. As an example, simulation and measurement results are given for the input stage of an automotive sensor interface. A good agreement is obtained from the lowest test frequency up to 1 GHz. Above this value, the measured results seem to be dominated by package effects.**

***Index Terms*—S-parameters, direct power injection (DPI), RF immunity, automotive EMC.**

## I. Introduction

Automotive modules (electronic subassemblies) need to pass many severe electromagnetic compatibility (EMC) tests before they can be integrated into a car. These so-called module-level tests are specified by the vehicle manufacturers (see e.g. [1], which can be freely downloaded from www.fordemc.com). In order to avoid failures, which could require expensive redesigns and increase total time-to-market, it is of utmost importance to predict the results of these tests in advance by means of accurate simulations.

As explained in [2], a correct prediction of the results of module-level radio frequency (RF) immunity tests, such as a bulk current injection (BCI) test [3] or an absorber-lined shielded enclosure (ALSE) test [4], is very challenging. Therefore, IC designers prefer to convert these unpredictable standards to more manageable IC-level ones, such as, e.g., a direct power injection (DPI) test [5] and to compare the results [6]. In [7], a first approach to perform such module-to-IC-level test conversion was presented, successfully translating a BCI test of a pressure sensor assembly to a DPI test. In order to model the IC-under-test, its scattering parameters (S-parameters) were measured. Obviously, such a measurement is only possible if engineering samples of the IC are available.

In this paper we propose to perform the conversion between the tests using simulated S-parameters of the investigated IC. In this way, module/IC-level requirements can be imposed on the circuit while it is still in its early design stage. We prove that proper simulation of the S-parameters of the IC-under-test in its normal operating point can accurately predict the measurement results, so that it is no longer needed to measure a prototype.

The paper is organized as follows. First, in Section II the principle of the module to IC-level test conversion is explained in detail. Second, in Section III a simulation method to obtain accurate S-parameters is described, which is based on the back-annotated analog schematics of the chip. The next section presents a measurement set-up, which makes use of a specially designed test board with external bias tees and direct current (DC) blocks that was used to validate the simulated data. Section V compares the results for the input stage of the automotive sensor interface described in [7]. Finally, in Section VI conclusions are drawn.

## II. Conversion of module-level to IC-level RF immunity requirements

In order to avoid unexpected failures of module-level EMC tests, it is appropriate to simulate these tests in advance [8], [9]. For RF immunity tests this becomes very challenging, because a normal model of the full set-up will either be too inaccurate (e.g. a lumped circuit model) or it will require an excessive amount of simulation time (e.g. a full-wave model). However, if the set-up is partitioned into subparts that are each modeled in their own appropriate way, an efficient model of the full set-up can be derived by properly combining all these sub-models in a high-level system model.

Once such a suitably partitioned system model has been set up, one is still faced with the challenge of deriving an adequate behavioral model of the chip (or chips) that is (are) part of the module. Ideally, this should be a nonlinear behavioral model that not only simulates the wanted functional and unwanted EMC behavior of the IC, but that is also efficient enough to be used in a higher-level simulation. However, although techniques have been developed already to derive

such models for circuit blocks such as voltage regulators (see [10], [11]), their extension to full chips would still be very laborious and time-consuming. Therefore, a more efficient alternative approach can be applied, where the module-level RF immunity requirements are translated into equivalent IC-level requirements. These equivalent conditions can be used then by the chip designers to optimize the chip architecture and design for its intended application. Fig. 1 illustrates the procedure.

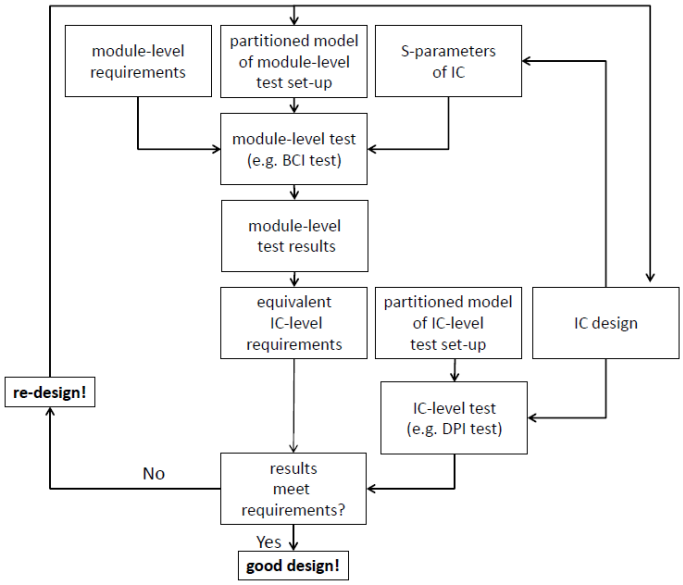



Fig. 1. Flowchart of module to IC level requirements conversion.

An IC design serves as a starting point in this flowchart. From the completed design of the IC its S-parameters are obtained by means of simulations (see Sec. III). These S-parameters are used then together with a partitioned model of the module-level test set-up and the EMC specifications to simulate the results of the module-level test, such as BCI. The results of this simulated test, being RF currents and voltages in case of the BCI test, are then used to calculate equivalent requirements for the IC-level test, which for the DPI test would be equivalent DPI power levels that the IC should be able to withstand. At the same time, the IC design is used together with the partitioned model of the IC-level set-up to simulate the results of the IC-level DPI test. If the obtained results meet the equivalent DPI levels (obtained from the BCI test results) it means that the IC is designed properly and would pass both IC and module-level tests. However, if the results do not comply with the equivalent IC-level requirements, the re-design of the IC and/or the module is needed.

Although this conversion has proven to be very useful and seems to be quite accurate, it is based on a few assumptions that have proven to be valid in many cases, but should be checked in each application of the proposed method. The first and most important assumption is that the IC is assumed to behave linearly as long as it meets the pass/fail criteria of the RF immunity test to be simulated. If that assumption holds, the nonlinear large-signal analysis can be replaced by a linear small-signal AC analysis so that the IC can be modeled by its S-parameters.

The second assumption concerns the conversion to equivalent DPI requirements. As already explained in [7], the equivalent DPI levels at each port (i.e. at each pin referenced to ground) can be easily derived from the calculated small-signal RF currents and voltages at each port of the S-parameter model. However, this means that all these DPI levels should be injected at the same time to have a full equivalence with the module-level test whereas in a standard DPI test [5] the pins are tested one-by-one. Hence our second assumption is that this does not make a lot of difference in most practical cases. Obviously, this is a weakness of our method that needs further study, but fortunately, if the IC-level tests are simulated, it should be fairly straightforward to apply the different calculated pin injections at the same time.

## III. Simulation of S-parameter IC models

A method was developed to calculate the S-parameters of an automotive IC. As a case study an input stage of an automotive sensor interface was used, which was described in detail in [7]. The technique consists of three steps, namely, (1) determination of the operating point, (2) determination of the chip-level S-parameters in this operating point, and (3) incorporation of the package effects.

The first two steps deal with the determination of the chip-level parameters and are quite time-consuming as the full chip needs to be simulated. On the contrary, the third step was very quick, because simple lumped models were applied to simulate the package.

In order to perform steps (1) and (2), a full chip model needs to be constructed. To do so, RC back-annotated circuit models were extracted for the analog blocks whereas Verilog behavioral models were used for the digital blocks. To further improve the accuracy of the model, simple models for the inductance of long metal connections and the substrate coupling between the pins-under-test were added. These “manual” circuit additions were necessary as they were not taken into account by our RC back-annotated schematics.

To complete the chip model (to be used in steps (1) and (2)), the requested S-parameter ports need to be added but one has to make sure (by using DC blocks or switches) that the $50\,\Omega$ impedances of these ports do not load the circuits in the first step. For this first step, a real operating point analysis did not work very well in the investigated cases. Therefore, a transient analysis was used to bring all circuits in the correct operating conditions (e.g. capacitors charged to the right levels, no circuits clipping, sample & holds set correctly) so that step (2) could be carried out. As this step (2) was just a small-signal AC analysis, it proved to be much more straightforward than step (1).

In the final step (3), package effects were added to the chip-level S-parameters obtained in the previous step. Similar to step (2), this is a very straightforward step as the S-parameter

model of the chip can be integrated in the package model very easily.

## IV. Measurement of S-parameter IC models

In order to measure S-parameters of ICs, a vector network analyzer is needed. In this work we used a 4-port Agilent E5071B ENA. To connect this instrument to the IC-under-test, our original idea was to use the DPI test board of the IC-under-test (see e.g. [12]), but we soon realized that it was better to use off-board DC blocks and bias tees instead of integrating them on the board such as in a DPI test board. In that way, the effect of these DC blocks and bias tees can be calibrated out and good $50\,\Omega$ connections can be made between the pins-under-test and their corresponding coaxial connectors.

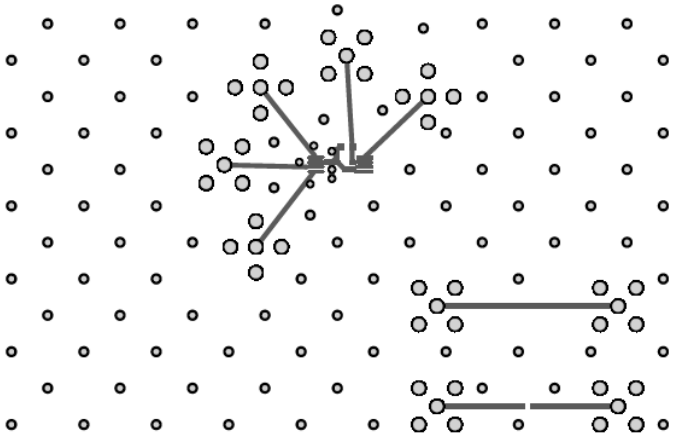


Fig. 2. Bottom layer of S-parameter test board.

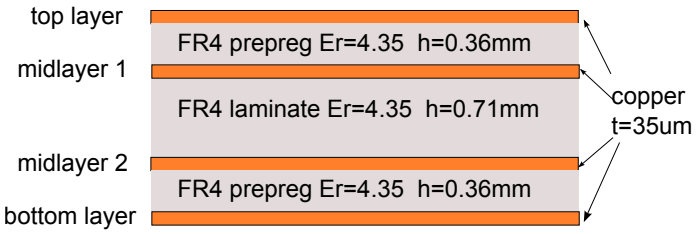


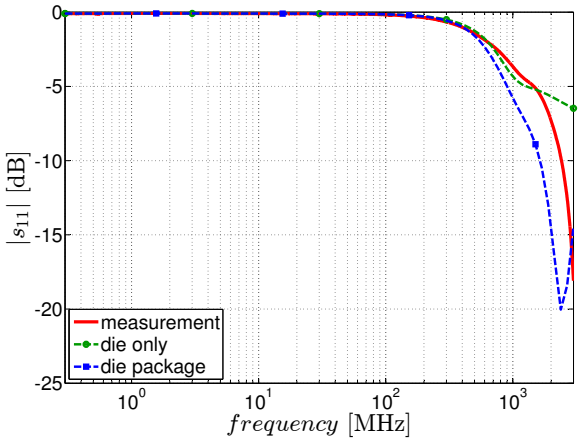

Fig. 3. Cross-section of the S-parameters board.

Fig. 2 shows the bottom side of the four-layer board, with a cross-section and substrate parameters depicted in Fig. 3, that was used to measure the results given in the next section. It is the same board that was also used to measure the S-parameters used in [7]. One can see five coaxial connectors with their connecting microstrip lines. This 5-port was measured by combining the results of three 4-port measurements into one $5\times5$ S-parameter matrix. However, only a $2\times2$ sub-matrix of it was used in the comparison with simulated results presented in this paper, because the other three pins were not really useful for this purpose as a decoupling capacitor (mounted on the top side of the board) was attached to them.

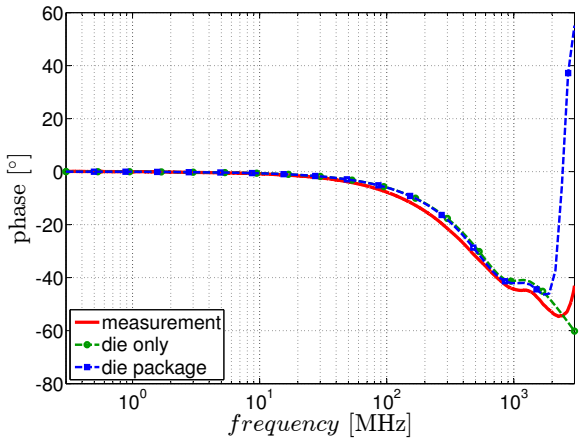
Prior to the actual measurements, the set-up was calibrated at the reference planes of the test board connectors. To eliminate the effect of the board, the reference planes were moved to the IC pins using port extensions. These port extensions were determined using the test structures that are also shown in Fig. 2. In all cases the test frequency range was 300 kHz (lowest test frequency of the Agilent E5071B) to 3 GHz (considered to be the maximum usable test frequency of the test board).

## V. Comparison of measured and simulated results

Figs. 4, 5 and 6 show both the measurement and simulation results for the two-port input stage of the ASIC described in [7]. Separate plots are shown for the amplitude (in dB) and phase (in degrees) of the $s_{11}$, $s_{22}$ and $s_{12}$ parameters. No results are shown for the $s_{21}$ parameter as it was nearly identical to the $s_{12}$ parameter.



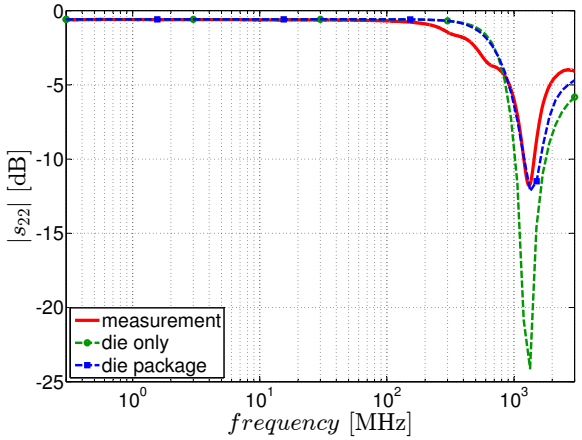

(a)



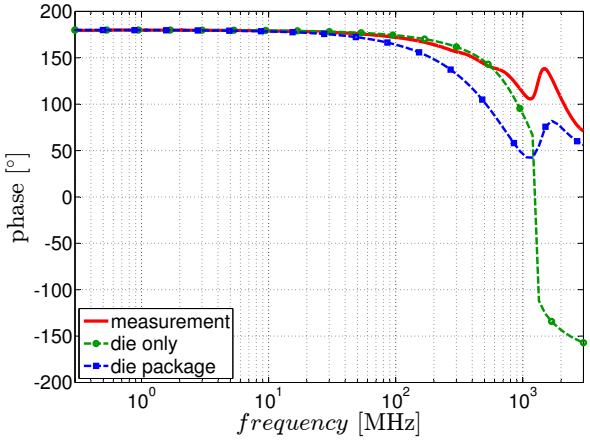

(b)

Fig. 4. Simulated and measured results for input reflection coefficient $s_{11}$ (a) amplitude (b) phase.

The total calculation time of steps (1) and (2) of the S-parameter simulations was 16 hours. All simulations were performed in Cadence Spectre, using a server with a 6-core 2.4 GHz CPU and with 98 GB of RAM. These chip-level

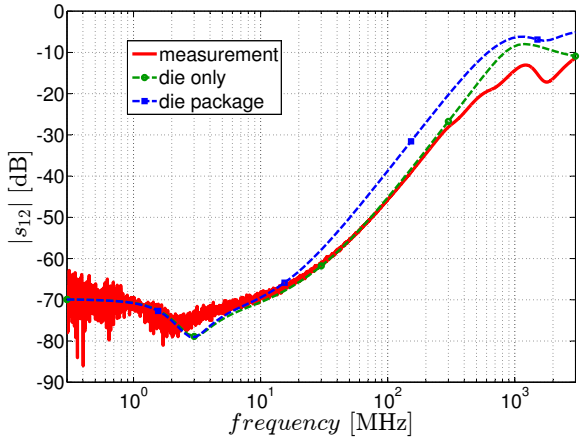



(a)

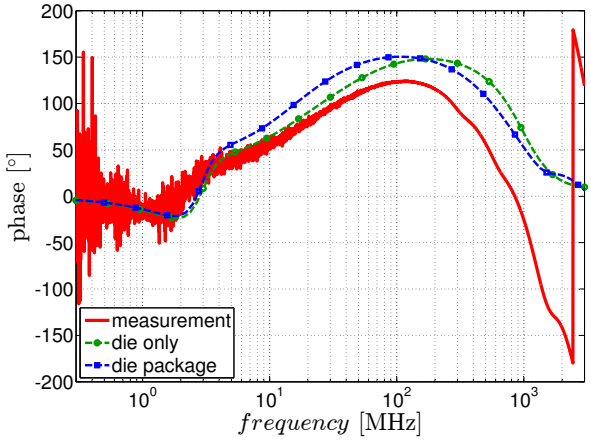



(b)

Fig. 5. Simulated and measured results for output reflection coefficient $s_{22}$ (a) amplitude (b) phase.




(a)




(b)

Fig. 6. Simulated and measured results for transmission coefficient $s_{12}$ (a) amplitude (b) phase.

results are represented in all figures by a green dashed line with circles (○), labeled as "die only". They are compared with an additional calculation result that includes package effects, plotted as dashed blue line with squares (□) and labeled "die package", and with the measurement results drawn with solid red line and labeled "measurement". The package model consisted of two 2 nH inductances (connected to the two input bond pads) and one 5 nH inductance (connected to the ground bond pad located at the other side of the die).

From the results depicted in Figs. 4, 5 and 6 it is clear that a good agreement between simulations and measurements is obtained up to 1 GHz. Above 1 GHz the correspondence starts to deteriorate quickly but could probably be improved by using more accurate package models.

## VI. Conclusions

In this paper, a method was proposed to transform the RF immunity requirements of automotive modules into equivalent IC-level requirements that can be applied to the ICs that are integrated in the modules. The conversion is based on a partitioned model of the full test set-up where the IC is modeled in its normal operating point by a linear S-parameter model obtained by means of simulations. In this way, the EMC behavior of the IC is validated when the circuit is still in its early design stage, before it has been taped-out. A good correspondence obtained between the simulated and measured S-parameters of the IC confirms the validity and usefulness of this approach.

## References

[1] *Electromagnetic compatibility specification for electrical/electronic components and subsystems*, Ford, EMC-CS-2009.1 Std., 2010.

[2] M. Coenen, H. Pues, and T. Bousquet, "Automotive RF immunity test set-up analysis: Why test results can't compare..." in *8th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Dubrovnik, Croatia, 6-9 Nov. 2011, pp. 71–75.

[3] *Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Bulk current injection (BCI)*, International Organization for Standardization, ISO 11452-4 Std., 2011.

[4] *Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 2: Absorber-lined shielded enclosure*, International Organization for Standardization, ISO 11452-2 Std., 2004.

[5] *Integrated Circuits - Measurement of Electromagnetic Immunity, 150 kHz to 1 GHz - Part 4: Measurement of Conducted Immunity - direct RF power injection method*, International Electrotechnical Commission, IEC 62132-4 Std., 2006.

[6] S. Miropolsky and S. Frei, "Comparability of RF immunity test methods for IC design purposes," in *8th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Dubrovnik, Croatia, 6-9 Nov. 2011, pp. 59–64.

[7] A. Durier, H. Pues, D. Vande Ginste, M. Chernobryvko, C. Gazda, and H. Rogier, "Novel modeling strategy for a BCI set-up applied in an automotive application: An industrial way to use EM simulation tools to help hardware and ASIC designers to improve their designs for immunity tests," in *8th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Dubrovnik, Croatia, 6-9 Nov. 2011, pp. 41–46.

[8] A. Alaeldine, R. Perdriau, M. Ramdani, J.-L. Levant, and M. Drissi, "A direct power injection model for immunity prediction in integrated circuits," *IEEE Transactions on Electromagnetic Compatibility*, vol. 50, no. 1, pp. 52–62, Feb. 2008.

[9] I. Chahine, M. Kadi, E. Gaboriaud, A. Louis, and B. Mazari, "Characterization and modeling of the susceptibility of integrated circuits to conducted electromagnetic disturbances up to 1 GHz," *IEEE Transactions on Electromagnetic Compatibility,*, vol. 50, no. 2, pp. 285–293, May 2008.

[10] C. Gazda, D. Vande Ginste, H. Rogier, I. Couckuyt, T. Dhaene, K. Stijnen, and H. Pues, "Harmonic Balance surrogate-based immunity modeling of a nonlinear analog circuit," *IEEE Transactions on Electromagnetic Compatibility, early access*, vol. -, pp. –, 2013.

[11] V. Ceperic and A. Baric, "Modelling of electromagnetic immunity of integrated circuits by artificial neural networks," in *20th International Zurich Symposium on Electromagnetic Compatibility*, Zurich, Switzerland, 12-16 Jan. 2009, pp. 373 –376.

[12] H. Pues and D. Pissoort, "Design of IEC 62132-4 compliant DPI test boards that work up to 2 GHz," in *International Symposium on Electromagnetic Compatibility (EMC EUROPE)*, Rome, Italy, 17-21 Sep. 2012, pp. 1–4.